

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 instruction tests for VRI-a instruction:
				5 *
				6 * E745 VREPI - Vector Replicate Immediate
				7 *
				8 * James Wekel February 2025
				9 *****
				11 *****
				12 *
				13 * basic instruction tests
				14 *
				15 *****
				16 * This program tests proper functioning of the z/arch E7 VRI-a
				17 * Vector Replicate Immediate instruction.
				18 * Exceptions are not tested.
				19 *
				20 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				21 * obvious coding errors. None of the tests are thorough. They are
				22 * NOT designed to test all aspects of any of the instructions.
				23 *
				24 *****
				25 *
				26 * *Testcase zvector-e7-21-VREPI
				27 * *
				28 * * Zvector E7 instruction tests for VRI-a instruction:
				29 * *
				30 * * E745 VREPI - Vector Replicate Immediate
				31 * *
				32 * * # -----
				33 * * # This tests only the basic function of the instruction.
				34 * * # Exceptions are NOT tested.
				35 * * # -----
				36 * *
				37 * main size 2
				38 * numcpu 1
				39 * sysclear
				40 * archlvl z/Arch
				41 * *
				42 * loadcore "\$(testpath)/zvector-e7-21-VREPI.core" 0x0
				43 * *
				44 * diag8cmd enable # (needed for messages to Hercules console)
				45 * runtest 5
				46 * diag8cmd disable # (reset back to default)
				47 * *
				48 * *Done
				49 * *
				50 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				52 *****
				53 * FCHECK Macro - Is a Facility Bit set?
				54 *
				55 * If the facility bit is NOT set, an message is issued and
				56 * the test is skipped.
				57 *
				58 * Fcheck uses R0, R1 and R2
				59 *
				60 * eg. FCHECK 134, 'vector-packed-decimal'
				61 *****
				62 MACRO
				63 FCHECK &BITNO, &NOTSETMSG
				64 . * &BITNO : facility bit number to check
				65 . * &NOTSETMSG : 'facility name'
				66 LCLA &FBBYTE Facility bit in Byte
				67 LCLA &FBBIT Facility bit within Byte
				68
				69 LCLA &L(8)
				70 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				71
				72 &FBBYTE SETA &BITNO/8
				73 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				74 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				75
				76 B X&SYSNDX
				77 * Fcheck data area
				78 * skip messgae
				79 SKT&SYSNDX DC C' Skipping tests: '
				80 DC C&NOTSETMSG
				81 DC C' (bit &BITNO) is not installed.'
				82 SKL&SYSNDX EQU *-SKT&SYSNDX
				83 * facility bits
				84 DS FD gap
				85 FB&SYSNDX DS 4FD
				86 DS FD gap
				87 *
				88 X&SYSNDX EQU *
				89 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				90 STFLE FB&SYSNDX get facility bits
				91
				92 XGR R0, R0
				93 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				94 N R0, =F' &FBBIT' is bit set?
				95 BNZ XC&SYSNDX
				96 *
				97 * facility bit not set, issue message and exit
				98 *
				99 LA R0, SKL&SYSNDX message length
				100 LA R1, SKT&SYSNDX message address
				101 BAL R2, MSG
				102
				103 B EOJ
				104 XC&SYSNDX EQU *
				105 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				107	*****
				108	* Low core PSWs
				109	*****
00000000		00000000	0000219F	110	ZVE7TST START 0
		00000000		111	USING ZVE7TST, R0 Low core addressability
		00000140	00000000	112	
				113	SVOLDPSW EQU ZVE7TST+X' 140' z/Arch Supervisor call old PSW
00000000		00000000	000001A0	115	ORG ZVE7TST+X' 1A0' z/Architecture RESTART PSW
000001A0	00000001 80000000			116	DC X' 0000000180000000'
000001A8	00000000 00000200			117	DC AD(BEGIN)
000001B0		000001B0	000001D0	119	ORG ZVE7TST+X' 1D0' z/Architecture PROGRAM CHECK PSW
000001D0	00020001 80000000			120	DC X' 0002000180000000'
000001D8	00000000 0000DEAD			121	DC AD(X' DEAD')
000001E0		000001E0	00000200	123	ORG ZVE7TST+X' 200' Start of actual test program..
				125	*****
				126	* The actual "ZVE7TST" program itself...
				127	*****
				128	*
				129	* Architecture Mode: z/Arch
				130	* Register Usage:
				131	*
				132	* R0 (work)
				133	* R1- 4 (work)
				134	* R5 Testing control table - current test base
				135	* R6- R7 (work)
				136	* R8 First base register
				137	* R9 Second base register
				138	* R10 Third base register
				139	* R11 E7TEST call return
				140	* R12 E7TESTS register
				141	* R13 (work)
				142	* R14 Subroutine call
				143	* R15 Secondary Subroutine call or work
				144	*
				145	*****
00000200		00000200		147	USING BEGIN, R8 FIRST Base Register
00000200		00001200		148	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		149	USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			151	BEGIN BALR R8, 0 Inititalize FIRST base register
00000202	0680			152	BCTR R8, 0 Inititalize FIRST base register
00000204	0680			153	BCTR R8, 0 Inititalize FIRST base register
00000206	4190 8800		00000800	155	LA R9, 2048(, R8) Inititalize SECOND base register
0000020A	4190 9800		00000800	156	LA R9, 2048(, R9) Inititalize SECOND base register
				157	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				349	*****
				350	* Normal completion or Abnormal termination PSWs
				351	*****
00000498	00020001 80000000			353	E0JPSW DC 0D' 0' , X' 0002000180000000' , AD(0)
000004A8	B2B2 8298		00000498	355	E0J LPSWE E0JPSW Normal completion
000004B0	00020001 80000000			357	FAILPSW DC 0D' 0' , X' 0002000180000000' , AD(X' BAD')
000004C0	B2B2 82B0		000004B0	359	FAILTEST LPSWE FAILPSW Abnormal termination
				361	*****
				362	* Working Storage
				363	*****
000004C4	00000000			365	CTLRO DS F CRO
000004C8	00000000			366	DS F
000004CC				368	LTORG , Literals pool
000004CC	00000040			369	=F' 64'
000004D0	000020FC			370	=A(E7TESTS)
000004D4	00000001			371	=F' 1'
000004D8	0000			372	=H' 0'
000004DA	005F			373	=AL2(L' MSGMSG)
000004DC	4E			374	=C' '+'
000004DD	40			375	=C' ' '
000004DE	60			376	=C' - ' '
				377	
				378	* some constants
				379	
	00000400	00000001		380	K EQU 1024 One KB
	00001000	00000001		381	PAGE EQU (4*K) Size of one page
	00010000	00000001		382	K64 EQU (64*K) 64 KB
	00100000	00000001		383	MB EQU (K*K) 1 MB
				384	
	AABBCCDD	00000001		385	REG2PATT EQU X' AABBCCDD' Polluted Register pattern
	000000DD	00000001		386	REG2LOW EQU X' DD' (last byte above)

[illegible]

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				432	*****
				433	* E7TEST DSECT
				434	*****
				436	E7TEST DSECT ,
00000000	00000000			437	TSUB DC A(0) pointer to test
00000004	0000			438	TNUM DC H' 00' Test Number
00000006	00			439	DC X' 00'
				440	
00000007	00			441	M3 DC HL1' 00' m3 field
00000008	0000			442	I2 DC XL2' 00' i2 used
				443	
0000000A	40404040	40404040		444	OPNAME DC CL8' ' E7 name
00000014	00000000			445	V2ADDR DC A(0) address of v2 source
00000018	00000000			446	V3ADDR DC A(0) address of v3 source
0000001C	00000000			447	RELEN DC A(0) RESULT LENGTH
00000020	00000000			448	READDR DC A(0) result (expected) address
00000028	00000000	00000000		449	DS FD gap
00000030	00000000	00000000		450	V10UTPUT DS XL16 V1 Output
00000040	00000000	00000000		451	DS FD gap
				452	
				453	* test routine will be here (from VRI-a macro)
				454	*
				455	* followed by
				456	* EXPECTED RESULT
				458	ZVE7TST CSECT ,
000010C4		00000000	0000219F	459	DS 0F
				461	*****
				462	* Macros to help build test tables
				463	*****
				465	*
				466	* macros to generate individual test
				467	*
				468	MACRO
				469	VRI_A &INST, &I2, &M3
				470	. * &INST - VRI-a instruction under test
				471	. * &i2 - i2 field (signed decimal)
				472	. * &m3 - element size
				473	
				474	GBLA &TNUM
				475	&TNUM SETA &TNUM+1
				476	
				477	DS 0FD
				478	USING *, R5 base for test data and test routine
				479	
				480	T&TNUM DC A(X&TNUM) address of test routine
				481	DC H' &TNUM test number
				482	DC X' 00'

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				530 *****	
				531 * E7 VRI-a tests	
				532 *****	
				533 PRINT DATA	
				534 *	
				535 * E745 VREPI - Vector Replicate Immediate	
				536 *	
				537 * VRI_A instruction, I2 (signed decimal), M3	
				538 * followed by	
				539 * 16 byte expected result (V1)	
				540 *-----	
				541 * VREPI - Vector Replicate Immediate	
				542 *-----	
				543 *Byte	
				544 VRI_A VREPI, 0, 0	
000010C8				545+ DS OFD	
000010C8		000010C8		546+ USING *, R5	base for test data and test routine
000010C8	00001110			547+T1 DC A(X1)	address of test routine
000010CC	0001			548+ DC H' 1'	test number
000010CE	00			549+ DC X' 00'	
000010CF	00			550+ DC HL1' 0'	m3 field
000010D0	0000			551+ DC HL2' 0'	i2 used
000010D2	E5D9C5D7 C9404040			552+ DC CL8' VREPI'	instruction name
000010DC	00001134			553+ DC A(RE1+16)	address of v2 source
000010E0	00001144			554+ DC A(RE1+32)	address of v3 source
000010E4	00000010			555+ DC A(16)	result length
000010E8	00001124			556+REA1 DC A(RE1)	result address
000010F0	00000000 00000000			557+ DS FD	gap
000010F8	00000000 00000000			558+V101 DS XL16	V1 output
00001100	00000000 00000000				
00001108	00000000 00000000			559+ DS FD	gap
				560+*	
00001110				561+X1 DS OF	
00001110	E760 8EA4 0806		000010A4	562+ VL V22, V1FUDGE	
00001116	E760 0000 0845			563+ VREPI V22, 0, 0	test instruction (dest is a source)
0000111C	E760 5030 080E		000010F8	564+ VST V22, V101	save v1 output
00001122	07FB			565+ BR R11	return
00001124				566+RE1 DC OF	xl16 expected result
00001124				567+ DROP R5	
00001124	00000000 00000000			568 DC 16HL1' 0'	result
0000112C	00000000 00000000				
				569	
				570 VRI_A VREPI, 1, 0	
00001138				571+ DS OFD	
00001138		00001138		572+ USING *, R5	base for test data and test routine
00001138	00001180			573+T2 DC A(X2)	address of test routine
0000113C	0002			574+ DC H' 2'	test number
0000113E	00			575+ DC X' 00'	
0000113F	00			576+ DC HL1' 0'	m3 field
00001140	0001			577+ DC HL2' 1'	i2 used
00001142	E5D9C5D7 C9404040			578+ DC CL8' VREPI'	instruction name
0000114C	000011A4			579+ DC A(RE2+16)	address of v2 source
00001150	000011B4			580+ DC A(RE2+32)	address of v3 source
00001154	00000010			581+ DC A(16)	result length
00001158	00001194			582+REA2 DC A(RE2)	result address
00001160	00000000 00000000			583+ DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001168	00000000 00000000			584+V102	DS	XL16	V1 output
00001170	00000000 00000000						
00001178	00000000 00000000			585+ 586+*	DS	FD	gap
00001180				587+X2	DS	0F	
00001180	E760 8EA4 0806		000010A4	588+	VL	V22, V1FUDGE	
00001186	E760 0001 0845			589+	VREPI	V22, 1, 0	test instruction (dest is a source)
0000118C	E760 5030 080E		00001168	590+	VST	V22, V102	save v1 output
00001192	07FB			591+	BR	R11	return
00001194				592+RE2	DC	0F	xl16 expected result
00001194				593+	DROP	R5	
00001194	01010101 01010101			594	DC	16HL1' 1'	result
0000119C	01010101 01010101						
				595			
000011A8				596	VRI_A	VREPI, 2, 0	
000011A8		000011A8		597+	DS	0FD	
000011A8	000011F0			598+	USING	*, R5	base for test data and test routine
000011AC	0003			599+T3	DC	A(X3)	address of test routine
000011AE	00			600+	DC	H' 3'	test number
000011AF	00			601+	DC	X' 00'	
000011B0	0002			602+	DC	HL1' 0'	m3 field
000011B2	E5D9C5D7 C9404040			603+	DC	HL2' 2'	i2 used
000011BC	00001214			604+	DC	CL8' VREPI'	instruction name
000011C0	00001224			605+	DC	A(RE3+16)	address of v2 source
000011C4	00000010			606+	DC	A(RE3+32)	address of v3 source
000011C8	00001204			607+	DC	A(16)	result length
000011D0	00000000 00000000			608+REA3	DC	A(RE3)	result address
000011D8	00000000 00000000			609+	DS	FD	gap
000011E0	00000000 00000000			610+V103	DS	XL16	V1 output
000011E8	00000000 00000000						
				611+	DS	FD	gap
				612+*			
000011F0				613+X3	DS	0F	
000011F0	E760 8EA4 0806		000010A4	614+	VL	V22, V1FUDGE	
000011F6	E760 0002 0845			615+	VREPI	V22, 2, 0	test instruction (dest is a source)
000011FC	E760 5030 080E		000011D8	616+	VST	V22, V103	save v1 output
00001202	07FB			617+	BR	R11	return
00001204				618+RE3	DC	0F	xl16 expected result
00001204				619+	DROP	R5	
00001204	02020202 02020202			620	DC	16HL1' 2'	result
0000120C	02020202 02020202						
				621			
00001218				622	VRI_A	VREPI, 99, 0	
00001218		00001218		623+	DS	0FD	
00001218	00001260			624+	USING	*, R5	base for test data and test routine
0000121C	0004			625+T4	DC	A(X4)	address of test routine
0000121E	00			626+	DC	H' 4'	test number
0000121F	00			627+	DC	X' 00'	
00001220	0063			628+	DC	HL1' 0'	m3 field
00001222	E5D9C5D7 C9404040			629+	DC	HL2' 99'	i2 used
0000122C	00001284			630+	DC	CL8' VREPI'	instruction name
00001230	00001294			631+	DC	A(RE4+16)	address of v2 source
00001234	00000010			632+	DC	A(RE4+32)	address of v3 source
00001238	00001274			633+	DC	A(16)	result length
00001240	00000000 00000000			634+REA4	DC	A(RE4)	result address
				635+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001248	00000000 00000000			636+V104	DS	XL16	V1 output
00001250	00000000 00000000						
00001258	00000000 00000000			637+ 638+*	DS	FD	gap
00001260				639+X4	DS	OF	
00001260	E760 8EA4 0806		000010A4	640+	VL	V22, V1FUDGE	
00001266	E760 0063 0845			641+	VREPI	V22, 99, 0	test instruction (dest is a source)
0000126C	E760 5030 080E		00001248	642+	VST	V22, V104	save v1 output
00001272	07FB			643+	BR	R11	return
00001274				644+RE4	DC	OF	xl16 expected result
00001274				645+	DROP	R5	
00001274	63636363 63636363			646	DC	16HL1' 99'	result
0000127C	63636363 63636363						
				647			
				648	VRI_A	VREPI, 999, 0	
00001288				649+	DS	OFD	
00001288		00001288		650+	USING	*, R5	base for test data and test routine
00001288	000012D0			651+T5	DC	A(X5)	address of test routine
0000128C	0005			652+	DC	H' 5'	test number
0000128E	00			653+	DC	X' 00'	
0000128F	00			654+	DC	HL1' 0'	m3 field
00001290	03E7			655+	DC	HL2' 999'	i2 used
00001292	E5D9C5D7 C9404040			656+	DC	CL8' VREPI'	instruction name
0000129C	000012F4			657+	DC	A(RE5+16)	address of v2 source
000012A0	00001304			658+	DC	A(RE5+32)	address of v3 source
000012A4	00000010			659+	DC	A(16)	result length
000012A8	000012E4			660+REA5	DC	A(RE5)	result address
000012B0	00000000 00000000			661+	DS	FD	gap
000012B8	00000000 00000000			662+V105	DS	XL16	V1 output
000012C0	00000000 00000000						
000012C8	00000000 00000000			663+ 664+*	DS	FD	gap
				665+X5	DS	OF	
000012D0				666+	VL	V22, V1FUDGE	
000012D0	E760 8EA4 0806		000010A4	667+	VREPI	V22, 999, 0	test instruction (dest is a source)
000012D6	E760 03E7 0845			668+	VST	V22, V105	save v1 output
000012DC	E760 5030 080E		000012B8	669+	BR	R11	return
000012E2	07FB			670+RE5	DC	OF	xl16 expected result
000012E4				671+	DROP	R5	
000012E4	E7E7E7E7 E7E7E7E7			672	DC	16HL1' 999'	result
000012EC	E7E7E7E7 E7E7E7E7						
				673			
				674	VRI_A	VREPI, - 1, 0	
000012F8				675+	DS	OFD	
000012F8		000012F8		676+	USING	*, R5	base for test data and test routine
000012F8	00001340			677+T6	DC	A(X6)	address of test routine
000012FC	0006			678+	DC	H' 6'	test number
000012FE	00			679+	DC	X' 00'	
000012FF	00			680+	DC	HL1' 0'	m3 field
00001300	FFFF			681+	DC	HL2' - 1'	i2 used
00001302	E5D9C5D7 C9404040			682+	DC	CL8' VREPI'	instruction name
0000130C	00001364			683+	DC	A(RE6+16)	address of v2 source
00001310	00001374			684+	DC	A(RE6+32)	address of v3 source
00001314	00000010			685+	DC	A(16)	result length
00001318	00001354			686+REA6	DC	A(RE6)	result address
00001320	00000000 00000000			687+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001328	00000000 00000000			688+V106	DS	XL16	V1 output
00001330	00000000 00000000						
00001338	00000000 00000000			689+ 690+*	DS	FD	gap
00001340				691+X6	DS	0F	
00001340	E760 8EA4 0806		000010A4	692+	VL	V22, V1FUDGE	
00001346	E760 FFFF 0845			693+	VREPI	V22, -1, 0	test instruction (dest is a source)
0000134C	E760 5030 080E		00001328	694+	VST	V22, V106	save v1 output
00001352	07FB			695+	BR	R11	return
00001354				696+RE6	DC	0F	xl16 expected result
00001354				697+	DROP	R5	
00001354	FFFFFFFF FFFFFFFF			698	DC	16HL1' - 1'	result
0000135C	FFFFFFFF FFFFFFFF						
				699			
				700			
00001368				701+	VRI_A	VREPI, -22, 0	
00001368		00001368		702+	DS	0FD	
00001368	000013B0			703+T7	USING	*, R5	base for test data and test routine
0000136C	0007			704+	DC	A(X7)	address of test routine
0000136E	00			705+	DC	H' 7'	test number
0000136F	00			706+	DC	X' 00'	
00001370	FFEA			707+	DC	HL1' 0'	m3 field
00001372	E5D9C5D7 C9404040			708+	DC	HL2' - 22'	i2 used
0000137C	000013D4			709+	DC	CL8' VREPI'	instruction name
00001380	000013E4			710+	DC	A(RE7+16)	address of v2 source
00001384	00000010			711+	DC	A(RE7+32)	address of v3 source
00001388	000013C4			712+REA7	DC	A(16)	result length
00001390	00000000 00000000			713+	DC	A(RE7)	result address
00001398	00000000 00000000			714+V107	DS	FD	gap
000013A0	00000000 00000000				DS	XL16	V1 output
000013A8	00000000 00000000			715+ 716+*	DS	FD	gap
000013B0				717+X7	DS	0F	
000013B0	E760 8EA4 0806		000010A4	718+	VL	V22, V1FUDGE	
000013B6	E760 FFEA 0845			719+	VREPI	V22, -22, 0	test instruction (dest is a source)
000013BC	E760 5030 080E		00001398	720+	VST	V22, V107	save v1 output
000013C2	07FB			721+	BR	R11	return
000013C4				722+RE7	DC	0F	xl16 expected result
000013C4				723+	DROP	R5	
000013C4	EAEAEAEA EAEAEAEA			724	DC	16HL1' - 22'	result
000013CC	EAEAEAEA EAEAEAEA						
				725			
				726			
000013D8				727+	VRI_A	VREPI, -302, 0	
000013D8		000013D8		728+	DS	0FD	
000013D8	00001420			729+T8	USING	*, R5	base for test data and test routine
000013DC	0008			730+	DC	A(X8)	address of test routine
000013DE	00			731+	DC	H' 8'	test number
000013DF	00			732+	DC	X' 00'	
000013E0	FED2			733+	DC	HL1' 0'	m3 field
000013E2	E5D9C5D7 C9404040			734+	DC	HL2' - 302'	i2 used
000013EC	00001444			735+	DC	CL8' VREPI'	instruction name
000013F0	00001454			736+	DC	A(RE8+16)	address of v2 source
000013F4	00000010			737+	DC	A(RE8+32)	address of v3 source
000013F8	00001434			738+REA8	DC	A(16)	result length
00001400	00000000 00000000			739+	DC	A(RE8)	result address
					DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001408	00000000 00000000			740+V108	DS	XL16	V1 output
00001410	00000000 00000000						
00001418	00000000 00000000			741+	DS	FD	gap
				742+*			
00001420				743+X8	DS	0F	
00001420	E760 8EA4 0806		000010A4	744+	VL	V22, V1FUDGE	
00001426	E760 FED2 0845			745+	VREPI	V22, -302, 0	test instruction (dest is a source)
0000142C	E760 5030 080E		00001408	746+	VST	V22, V108	save v1 output
00001432	07FB			747+	BR	R11	return
00001434				748+RE8	DC	0F	xl16 expected result
00001434				749+	DROP	R5	
00001434	D2D2D2D2 D2D2D2D2			750	DC	16HL1' -302'	result
0000143C	D2D2D2D2 D2D2D2D2						
				751			
				752 *Halfword			
				753	VRI_A	VREPI, 0, 1	
00001448				754+	DS	0FD	
00001448		00001448		755+	USING	*, R5	base for test data and test routine
00001448	00001490			756+T9	DC	A(X9)	address of test routine
0000144C	0009			757+	DC	H' 9'	test number
0000144E	00			758+	DC	X' 00'	
0000144F	01			759+	DC	HL1' 1'	m3 field
00001450	0000			760+	DC	HL2' 0'	i2 used
00001452	E5D9C5D7 C9404040			761+	DC	CL8' VREPI'	instruction name
0000145C	000014B4			762+	DC	A(RE9+16)	address of v2 source
00001460	000014C4			763+	DC	A(RE9+32)	address of v3 source
00001464	00000010			764+	DC	A(16)	result length
00001468	000014A4			765+REA9	DC	A(RE9)	result address
00001470	00000000 00000000			766+	DS	FD	gap
00001478	00000000 00000000			767+V109	DS	XL16	V1 output
00001480	00000000 00000000						
00001488	00000000 00000000			768+	DS	FD	gap
				769+*			
00001490				770+X9	DS	0F	
00001490	E760 8EA4 0806		000010A4	771+	VL	V22, V1FUDGE	
00001496	E760 0000 1845			772+	VREPI	V22, 0, 1	test instruction (dest is a source)
0000149C	E760 5030 080E		00001478	773+	VST	V22, V109	save v1 output
000014A2	07FB			774+	BR	R11	return
000014A4				775+RE9	DC	0F	xl16 expected result
000014A4				776+	DROP	R5	
000014A4	00000000 00000000			777	DC	8HL2' 0'	result
000014AC	00000000 00000000						
				778			
				779	VRI_A	VREPI, 1, 1	
000014B8				780+	DS	0FD	
000014B8		000014B8		781+	USING	*, R5	base for test data and test routine
000014B8	00001500			782+T10	DC	A(X10)	address of test routine
000014BC	000A			783+	DC	H' 10'	test number
000014BE	00			784+	DC	X' 00'	
000014BF	01			785+	DC	HL1' 1'	m3 field
000014C0	0001			786+	DC	HL2' 1'	i2 used
000014C2	E5D9C5D7 C9404040			787+	DC	CL8' VREPI'	instruction name
000014CC	00001524			788+	DC	A(RE10+16)	address of v2 source
000014D0	00001534			789+	DC	A(RE10+32)	address of v3 source
000014D4	00000010			790+	DC	A(16)	result length
000014D8	00001514			791+REA10	DC	A(RE10)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000014E0	00000000 00000000			792+	DS	FD	gap
000014E8	00000000 00000000			793+V1010	DS	XL16	V1 output
000014F0	00000000 00000000						
000014F8	00000000 00000000			794+	DS	FD	gap
				795+*			
00001500				796+X10	DS	0F	
00001500	E760 8EA4 0806		000010A4	797+	VL	V22, V1FUDGE	
00001506	E760 0001 1845			798+	VREPI	V22, 1, 1	test instruction (dest is a source)
0000150C	E760 5030 080E		000014E8	799+	VST	V22, V1010	save v1 output
00001512	07FB			800+	BR	R11	return
00001514				801+RE10	DC	0F	xl16 expected result
00001514				802+	DROP	R5	
00001514	00010001 00010001			803	DC	8HL2' 1'	result
0000151C	00010001 00010001						
				804			
				805	VRI_A	VREPI, 2, 1	
00001528				806+	DS	0FD	
00001528		00001528		807+	USING	*, R5	base for test data and test routine
00001528	00001570			808+T11	DC	A(X11)	address of test routine
0000152C	000B			809+	DC	H' 11'	test number
0000152E	00			810+	DC	X' 00'	
0000152F	01			811+	DC	HL1' 1'	m3 field
00001530	0002			812+	DC	HL2' 2'	i2 used
00001532	E5D9C5D7 C9404040			813+	DC	CL8' VREPI'	instruction name
0000153C	00001594			814+	DC	A(RE11+16)	address of v2 source
00001540	000015A4			815+	DC	A(RE11+32)	address of v3 source
00001544	00000010			816+	DC	A(16)	result length
00001548	00001584			817+REA11	DC	A(RE11)	result address
00001550	00000000 00000000			818+	DS	FD	gap
00001558	00000000 00000000			819+V1011	DS	XL16	V1 output
00001560	00000000 00000000						
00001568	00000000 00000000			820+	DS	FD	gap
				821+*			
00001570				822+X11	DS	0F	
00001570	E760 8EA4 0806		000010A4	823+	VL	V22, V1FUDGE	
00001576	E760 0002 1845			824+	VREPI	V22, 2, 1	test instruction (dest is a source)
0000157C	E760 5030 080E		00001558	825+	VST	V22, V1011	save v1 output
00001582	07FB			826+	BR	R11	return
00001584				827+RE11	DC	0F	xl16 expected result
00001584				828+	DROP	R5	
00001584	00020002 00020002			829	DC	8HL2' 2'	result
0000158C	00020002 00020002						
				830			
				831	VRI_A	VREPI, 99, 1	
00001598				832+	DS	0FD	
00001598		00001598		833+	USING	*, R5	base for test data and test routine
00001598	000015E0			834+T12	DC	A(X12)	address of test routine
0000159C	000C			835+	DC	H' 12'	test number
0000159E	00			836+	DC	X' 00'	
0000159F	01			837+	DC	HL1' 1'	m3 field
000015A0	0063			838+	DC	HL2' 99'	i2 used
000015A2	E5D9C5D7 C9404040			839+	DC	CL8' VREPI'	instruction name
000015AC	00001604			840+	DC	A(RE12+16)	address of v2 source
000015B0	00001614			841+	DC	A(RE12+32)	address of v3 source
000015B4	00000010			842+	DC	A(16)	result length
000015B8	000015F4			843+REA12	DC	A(RE12)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000015C0	00000000 00000000			844+	DS	FD	gap
000015C8	00000000 00000000			845+V1012	DS	XL16	V1 output
000015D0	00000000 00000000						
000015D8	00000000 00000000			846+	DS	FD	gap
				847+*			
000015E0				848+X12	DS	OF	
000015E0	E760 8EA4 0806		000010A4	849+	VL	V22, V1FUDGE	
000015E6	E760 0063 1845			850+	VREPI	V22, 99, 1	test instruction (dest is a source)
000015EC	E760 5030 080E		000015C8	851+	VST	V22, V1012	save v1 output
000015F2	07FB			852+	BR	R11	return
000015F4				853+RE12	DC	OF	xl16 expected result
000015F4				854+	DROP	R5	
000015F4	00630063 00630063			855	DC	8HL2' 99'	result
000015FC	00630063 00630063						
				856			
				857	VRI_A	VREPI, 9999, 1	
00001608				858+	DS	OFD	
00001608		00001608		859+	USING	*, R5	base for test data and test routine
00001608	00001650			860+T13	DC	A(X13)	address of test routine
0000160C	000D			861+	DC	H' 13'	test number
0000160E	00			862+	DC	X' 00'	
0000160F	01			863+	DC	HL1' 1'	m3 field
00001610	270F			864+	DC	HL2' 9999'	i2 used
00001612	E5D9C5D7 C9404040			865+	DC	CL8' VREPI'	instruction name
0000161C	00001674			866+	DC	A(RE13+16)	address of v2 source
00001620	00001684			867+	DC	A(RE13+32)	address of v3 source
00001624	00000010			868+	DC	A(16)	result length
00001628	00001664			869+REA13	DC	A(RE13)	result address
00001630	00000000 00000000			870+	DS	FD	gap
00001638	00000000 00000000			871+V1013	DS	XL16	V1 output
00001640	00000000 00000000						
00001648	00000000 00000000			872+	DS	FD	gap
				873+*			
00001650				874+X13	DS	OF	
00001650	E760 8EA4 0806		000010A4	875+	VL	V22, V1FUDGE	
00001656	E760 270F 1845			876+	VREPI	V22, 9999, 1	test instruction (dest is a source)
0000165C	E760 5030 080E		00001638	877+	VST	V22, V1013	save v1 output
00001662	07FB			878+	BR	R11	return
00001664				879+RE13	DC	OF	xl16 expected result
00001664				880+	DROP	R5	
00001664	270F270F 270F270F			881	DC	8HL2' 9999'	result
0000166C	270F270F 270F270F						
				882			
				883	VRI_A	VREPI, - 1, 1	
00001678				884+	DS	OFD	
00001678		00001678		885+	USING	*, R5	base for test data and test routine
00001678	000016C0			886+T14	DC	A(X14)	address of test routine
0000167C	000E			887+	DC	H' 14'	test number
0000167E	00			888+	DC	X' 00'	
0000167F	01			889+	DC	HL1' 1'	m3 field
00001680	FFFF			890+	DC	HL2' - 1'	i2 used
00001682	E5D9C5D7 C9404040			891+	DC	CL8' VREPI'	instruction name
0000168C	000016E4			892+	DC	A(RE14+16)	address of v2 source
00001690	000016F4			893+	DC	A(RE14+32)	address of v3 source
00001694	00000010			894+	DC	A(16)	result length
00001698	000016D4			895+REA14	DC	A(RE14)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000016A0	00000000 00000000			896+	DS	FD	gap
000016A8	00000000 00000000			897+V1014	DS	XL16	V1 output
000016B0	00000000 00000000						
000016B8	00000000 00000000			898+	DS	FD	gap
				899+*			
000016C0				900+X14	DS	OF	
000016C0	E760 8EA4 0806		000010A4	901+	VL	V22, V1FUDGE	
000016C6	E760 FFFF 1845			902+	VREPI	V22, - 1, 1	test instruction (dest is a source)
000016CC	E760 5030 080E		000016A8	903+	VST	V22, V1014	save v1 output
000016D2	07FB			904+	BR	R11	return
000016D4				905+RE14	DC	OF	xl16 expected result
000016D4				906+	DROP	R5	
000016D4	FFFFFFFF FFFFFFFF			907	DC	8HL2' - 1'	result
000016DC	FFFFFFFF FFFFFFFF						
				908			
				909	VRI_A	VREPI, - 2, 1	
000016E8				910+	DS	OFD	
000016E8		000016E8		911+	USING	*, R5	base for test data and test routine
000016E8	00001730			912+T15	DC	A(X15)	address of test routine
000016EC	000F			913+	DC	H' 15'	test number
000016EE	00			914+	DC	X' 00'	
000016EF	01			915+	DC	HL1' 1'	m3 field
000016F0	FFFE			916+	DC	HL2' - 2'	i2 used
000016F2	E5D9C5D7 C9404040			917+	DC	CL8' VREPI'	instruction name
000016FC	00001754			918+	DC	A(RE15+16)	address of v2 source
00001700	00001764			919+	DC	A(RE15+32)	address of v3 source
00001704	00000010			920+	DC	A(16)	result length
00001708	00001744			921+REA15	DC	A(RE15)	result address
00001710	00000000 00000000			922+	DS	FD	gap
00001718	00000000 00000000			923+V1015	DS	XL16	V1 output
00001720	00000000 00000000						
00001728	00000000 00000000			924+	DS	FD	gap
				925+*			
00001730				926+X15	DS	OF	
00001730	E760 8EA4 0806		000010A4	927+	VL	V22, V1FUDGE	
00001736	E760 FFFE 1845			928+	VREPI	V22, - 2, 1	test instruction (dest is a source)
0000173C	E760 5030 080E		00001718	929+	VST	V22, V1015	save v1 output
00001742	07FB			930+	BR	R11	return
00001744				931+RE15	DC	OF	xl16 expected result
00001744				932+	DROP	R5	
00001744	FFFEFFFE FFEFFFE			933	DC	8HL2' - 2'	result
0000174C	FFFEFFFE FFEFFFE						
				934			
				935	VRI_A	VREPI, - 22, 1	
00001758				936+	DS	OFD	
00001758		00001758		937+	USING	*, R5	base for test data and test routine
00001758	000017A0			938+T16	DC	A(X16)	address of test routine
0000175C	0010			939+	DC	H' 16'	test number
0000175E	00			940+	DC	X' 00'	
0000175F	01			941+	DC	HL1' 1'	m3 field
00001760	FFEA			942+	DC	HL2' - 22'	i2 used
00001762	E5D9C5D7 C9404040			943+	DC	CL8' VREPI'	instruction name
0000176C	000017C4			944+	DC	A(RE16+16)	address of v2 source
00001770	000017D4			945+	DC	A(RE16+32)	address of v3 source
00001774	00000010			946+	DC	A(16)	result length
00001778	000017B4			947+REA16	DC	A(RE16)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001780	00000000 00000000			948+	DS	FD	gap
00001788	00000000 00000000			949+V1016	DS	XL16	V1 output
00001790	00000000 00000000						
00001798	00000000 00000000			950+	DS	FD	gap
				951+*			
000017A0				952+X16	DS	OF	
000017A0	E760 8EA4 0806		000010A4	953+	VL	V22, V1FUDGE	
000017A6	E760 FFEA 1845			954+	VREPI	V22, - 22, 1	test instruction (dest is a source)
000017AC	E760 5030 080E		00001788	955+	VST	V22, V1016	save v1 output
000017B2	07FB			956+	BR	R11	return
000017B4				957+RE16	DC	OF	xl16 expected result
000017B4				958+	DROP	R5	
000017B4	FFEAFFEA FFEAFFEA			959	DC	8HL2' - 22'	result
000017BC	FFEAFFEA FFEAFFEA						
				960			
				961	VRI_A	VREPI, - 302, 1	
000017C8				962+	DS	OFD	
000017C8		000017C8		963+	USING	*, R5	base for test data and test routine
000017C8	00001810			964+T17	DC	A(X17)	address of test routine
000017CC	0011			965+	DC	H' 17'	test number
000017CE	00			966+	DC	X' 00'	
000017CF	01			967+	DC	HL1' 1'	m3 field
000017D0	FED2			968+	DC	HL2' - 302'	i2 used
000017D2	E5D9C5D7 C9404040			969+	DC	CL8' VREPI'	instruction name
000017DC	00001834			970+	DC	A(RE17+16)	address of v2 source
000017E0	00001844			971+	DC	A(RE17+32)	address of v3 source
000017E4	00000010			972+	DC	A(16)	result length
000017E8	00001824			973+REA17	DC	A(RE17)	result address
000017F0	00000000 00000000			974+	DS	FD	gap
000017F8	00000000 00000000			975+V1017	DS	XL16	V1 output
00001800	00000000 00000000						
00001808	00000000 00000000			976+	DS	FD	gap
				977+*			
00001810				978+X17	DS	OF	
00001810	E760 8EA4 0806		000010A4	979+	VL	V22, V1FUDGE	
00001816	E760 FED2 1845			980+	VREPI	V22, - 302, 1	test instruction (dest is a source)
0000181C	E760 5030 080E		000017F8	981+	VST	V22, V1017	save v1 output
00001822	07FB			982+	BR	R11	return
00001824				983+RE17	DC	OF	xl16 expected result
00001824				984+	DROP	R5	
00001824	FED2FED2 FED2FED2			985	DC	8HL2' - 302'	result
0000182C	FED2FED2 FED2FED2						
				986			
				987	VRI_A	VREPI, - 720, 1	
00001838				988+	DS	OFD	
00001838		00001838		989+	USING	*, R5	base for test data and test routine
00001838	00001880			990+T18	DC	A(X18)	address of test routine
0000183C	0012			991+	DC	H' 18'	test number
0000183E	00			992+	DC	X' 00'	
0000183F	01			993+	DC	HL1' 1'	m3 field
00001840	FD30			994+	DC	HL2' - 720'	i2 used
00001842	E5D9C5D7 C9404040			995+	DC	CL8' VREPI'	instruction name
0000184C	000018A4			996+	DC	A(RE18+16)	address of v2 source
00001850	000018B4			997+	DC	A(RE18+32)	address of v3 source
00001854	00000010			998+	DC	A(16)	result length
00001858	00001894			999+REA18	DC	A(RE18)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001860	00000000 00000000			1000+	DS	FD	gap
00001868	00000000 00000000			1001+V1018	DS	XL16	V1 output
00001870	00000000 00000000						
00001878	00000000 00000000			1002+	DS	FD	gap
				1003+*			
00001880				1004+X18	DS	OF	
00001880	E760 8EA4 0806		000010A4	1005+	VL	V22, V1FUDGE	
00001886	E760 FD30 1845			1006+	VREPI	V22, - 720, 1	test instruction (dest is a source)
0000188C	E760 5030 080E		00001868	1007+	VST	V22, V1018	save v1 output
00001892	07FB			1008+	BR	R11	return
00001894				1009+RE18	DC	OF	xl16 expected result
00001894				1010+	DROP	R5	
00001894	FD30FD30 FD30FD30			1011	DC	8HL2' - 720'	result
0000189C	FD30FD30 FD30FD30						
				1012			
				1013	VRI_A	VREPI, - 31456, 1	
000018A8				1014+	DS	OFD	
000018A8		000018A8		1015+	USING	*, R5	base for test data and test routine
000018A8	000018F0			1016+T19	DC	A(X19)	address of test routine
000018AC	0013			1017+	DC	H' 19'	test number
000018AE	00			1018+	DC	X' 00'	
000018AF	01			1019+	DC	HL1' 1'	m3 field
000018B0	8520			1020+	DC	HL2' - 31456'	i2 used
000018B2	E5D9C5D7 C9404040			1021+	DC	CL8' VREPI'	instruction name
000018BC	00001914			1022+	DC	A(RE19+16)	address of v2 source
000018C0	00001924			1023+	DC	A(RE19+32)	address of v3 source
000018C4	00000010			1024+	DC	A(16)	result length
000018C8	00001904			1025+REA19	DC	A(RE19)	result address
000018D0	00000000 00000000			1026+	DS	FD	gap
000018D8	00000000 00000000			1027+V1019	DS	XL16	V1 output
000018E0	00000000 00000000						
000018E8	00000000 00000000			1028+	DS	FD	gap
				1029+*			
000018F0				1030+X19	DS	OF	
000018F0	E760 8EA4 0806		000010A4	1031+	VL	V22, V1FUDGE	
000018F6	E760 8520 1845			1032+	VREPI	V22, - 31456, 1	test instruction (dest is a source)
000018FC	E760 5030 080E		000018D8	1033+	VST	V22, V1019	save v1 output
00001902	07FB			1034+	BR	R11	return
00001904				1035+RE19	DC	OF	xl16 expected result
00001904				1036+	DROP	R5	
00001904	85208520 85208520			1037	DC	8HL2' - 31456'	result
0000190C	85208520 85208520						
				1038			
				1039 *Word			
				1040	VRI_A	VREPI, 0, 2	
00001918				1041+	DS	OFD	
00001918		00001918		1042+	USING	*, R5	base for test data and test routine
00001918	00001960			1043+T20	DC	A(X20)	address of test routine
0000191C	0014			1044+	DC	H' 20'	test number
0000191E	00			1045+	DC	X' 00'	
0000191F	02			1046+	DC	HL1' 2'	m3 field
00001920	0000			1047+	DC	HL2' 0'	i2 used
00001922	E5D9C5D7 C9404040			1048+	DC	CL8' VREPI'	instruction name
0000192C	00001984			1049+	DC	A(RE20+16)	address of v2 source
00001930	00001994			1050+	DC	A(RE20+32)	address of v3 source
00001934	00000010			1051+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001938	00001974			1052+REA20	DC	A(RE20)	result address
00001940	00000000 00000000			1053+	DS	FD	gap
00001948	00000000 00000000			1054+V1020	DS	XL16	V1 output
00001950	00000000 00000000						
00001958	00000000 00000000			1055+	DS	FD	gap
				1056+*			
00001960				1057+X20	DS	0F	
00001960	E760 8EA4 0806		000010A4	1058+	VL	V22, V1FUDGE	
00001966	E760 0000 2845			1059+	VREPI	V22, 0, 2	test instruction (dest is a source)
0000196C	E760 5030 080E		00001948	1060+	VST	V22, V1020	save v1 output
00001972	07FB			1061+	BR	R11	return
00001974				1062+RE20	DC	0F	xl16 expected result
00001974				1063+	DROP	R5	
00001974	00000000 00000000			1064	DC	4FL4' 0'	result
0000197C	00000000 00000000						
				1065			
				1066	VRI_A	VREPI, 1, 2	
00001988				1067+	DS	0FD	
00001988		00001988		1068+	USING	*, R5	base for test data and test routine
00001988	000019D0			1069+T21	DC	A(X21)	address of test routine
0000198C	0015			1070+	DC	H' 21'	test number
0000198E	00			1071+	DC	X' 00'	
0000198F	02			1072+	DC	HL1' 2'	m3 field
00001990	0001			1073+	DC	HL2' 1'	i2 used
00001992	E5D9C5D7 C9404040			1074+	DC	CL8' VREPI'	instruction name
0000199C	000019F4			1075+	DC	A(RE21+16)	address of v2 source
000019A0	00001A04			1076+	DC	A(RE21+32)	address of v3 source
000019A4	00000010			1077+	DC	A(16)	result length
000019A8	000019E4			1078+REA21	DC	A(RE21)	result address
000019B0	00000000 00000000			1079+	DS	FD	gap
000019B8	00000000 00000000			1080+V1021	DS	XL16	V1 output
000019C0	00000000 00000000						
000019C8	00000000 00000000			1081+	DS	FD	gap
				1082+*			
000019D0				1083+X21	DS	0F	
000019D0	E760 8EA4 0806		000010A4	1084+	VL	V22, V1FUDGE	
000019D6	E760 0001 2845			1085+	VREPI	V22, 1, 2	test instruction (dest is a source)
000019DC	E760 5030 080E		000019B8	1086+	VST	V22, V1021	save v1 output
000019E2	07FB			1087+	BR	R11	return
000019E4				1088+RE21	DC	0F	xl16 expected result
000019E4				1089+	DROP	R5	
000019E4	00000001 00000001			1090	DC	4FL4' 1'	result
000019EC	00000001 00000001						
				1091			
				1092	VRI_A	VREPI, 2, 2	
000019F8				1093+	DS	0FD	
000019F8		000019F8		1094+	USING	*, R5	base for test data and test routine
000019F8	00001A40			1095+T22	DC	A(X22)	address of test routine
000019FC	0016			1096+	DC	H' 22'	test number
000019FE	00			1097+	DC	X' 00'	
000019FF	02			1098+	DC	HL1' 2'	m3 field
00001A00	0002			1099+	DC	HL2' 2'	i2 used
00001A02	E5D9C5D7 C9404040			1100+	DC	CL8' VREPI'	instruction name
00001A0C	00001A64			1101+	DC	A(RE22+16)	address of v2 source
00001A10	00001A74			1102+	DC	A(RE22+32)	address of v3 source
00001A14	00000010			1103+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001A18	00001A54			1104+REA22	DC	A(RE22)	result address
00001A20	00000000 00000000			1105+	DS	FD	gap
00001A28	00000000 00000000			1106+V1022	DS	XL16	V1 output
00001A30	00000000 00000000						
00001A38	00000000 00000000			1107+	DS	FD	gap
				1108+*			
00001A40				1109+X22	DS	0F	
00001A40	E760 8EA4 0806		000010A4	1110+	VL	V22, V1FUDGE	
00001A46	E760 0002 2845			1111+	VREPI	V22, 2, 2	test instruction (dest is a source)
00001A4C	E760 5030 080E		00001A28	1112+	VST	V22, V1022	save v1 output
00001A52	07FB			1113+	BR	R11	return
00001A54				1114+RE22	DC	0F	xl16 expected result
00001A54				1115+	DROP	R5	
00001A54	00000002 00000002			1116	DC	4FL4' 2'	result
00001A5C	00000002 00000002						
				1117			
				1118	VRI_A	VREPI, 99, 2	
00001A68				1119+	DS	0FD	
00001A68		00001A68		1120+	USING	*, R5	base for test data and test routine
00001A68	00001AB0			1121+T23	DC	A(X23)	address of test routine
00001A6C	0017			1122+	DC	H' 23'	test number
00001A6E	00			1123+	DC	X' 00'	
00001A6F	02			1124+	DC	HL1' 2'	m3 field
00001A70	0063			1125+	DC	HL2' 99'	i2 used
00001A72	E5D9C5D7 C9404040			1126+	DC	CL8' VREPI'	instruction name
00001A7C	00001AD4			1127+	DC	A(RE23+16)	address of v2 source
00001A80	00001AE4			1128+	DC	A(RE23+32)	address of v3 source
00001A84	00000010			1129+	DC	A(16)	result length
00001A88	00001AC4			1130+REA23	DC	A(RE23)	result address
00001A90	00000000 00000000			1131+	DS	FD	gap
00001A98	00000000 00000000			1132+V1023	DS	XL16	V1 output
00001AA0	00000000 00000000						
00001AA8	00000000 00000000			1133+	DS	FD	gap
				1134+*			
00001AB0				1135+X23	DS	0F	
00001AB0	E760 8EA4 0806		000010A4	1136+	VL	V22, V1FUDGE	
00001AB6	E760 0063 2845			1137+	VREPI	V22, 99, 2	test instruction (dest is a source)
00001ABC	E760 5030 080E		00001A98	1138+	VST	V22, V1023	save v1 output
00001AC2	07FB			1139+	BR	R11	return
00001AC4				1140+RE23	DC	0F	xl16 expected result
00001AC4				1141+	DROP	R5	
00001AC4	00000063 00000063			1142	DC	4FL4' 99'	result
00001ACC	00000063 00000063						
				1143			
				1144	VRI_A	VREPI, 9999, 2	
00001AD8				1145+	DS	0FD	
00001AD8		00001AD8		1146+	USING	*, R5	base for test data and test routine
00001AD8	00001B20			1147+T24	DC	A(X24)	address of test routine
00001ADC	0018			1148+	DC	H' 24'	test number
00001ADE	00			1149+	DC	X' 00'	
00001ADF	02			1150+	DC	HL1' 2'	m3 field
00001AE0	270F			1151+	DC	HL2' 9999'	i2 used
00001AE2	E5D9C5D7 C9404040			1152+	DC	CL8' VREPI'	instruction name
00001AEC	00001B44			1153+	DC	A(RE24+16)	address of v2 source
00001AF0	00001B54			1154+	DC	A(RE24+32)	address of v3 source
00001AF4	00000010			1155+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001AF8	00001B34			1156+REA24	DC	A(RE24)	result address
00001B00	00000000 00000000			1157+	DS	FD	gap
00001B08	00000000 00000000			1158+V1024	DS	XL16	V1 output
00001B10	00000000 00000000						
00001B18	00000000 00000000			1159+	DS	FD	gap
				1160+*			
00001B20				1161+X24	DS	0F	
00001B20	E760 8EA4 0806		000010A4	1162+	VL	V22, V1FUDGE	
00001B26	E760 270F 2845			1163+	VREPI	V22, 9999, 2	test instruction (dest is a source)
00001B2C	E760 5030 080E		00001B08	1164+	VST	V22, V1024	save v1 output
00001B32	07FB			1165+	BR	R11	return
00001B34				1166+REA24	DC	0F	xl16 expected result
00001B34				1167+	DROP	R5	
00001B34	0000270F 0000270F			1168	DC	4FL4' 9999'	result
00001B3C	0000270F 0000270F						
				1169			
				1170	VRI_A	VREPI, - 1, 2	
00001B48				1171+	DS	0FD	
00001B48		00001B48		1172+	USING	*, R5	base for test data and test routine
00001B48	00001B90			1173+T25	DC	A(X25)	address of test routine
00001B4C	0019			1174+	DC	H' 25'	test number
00001B4E	00			1175+	DC	X' 00'	
00001B4F	02			1176+	DC	HL1' 2'	m3 field
00001B50	FFFF			1177+	DC	HL2' - 1'	i2 used
00001B52	E5D9C5D7 C9404040			1178+	DC	CL8' VREPI'	instruction name
00001B5C	00001BB4			1179+	DC	A(RE25+16)	address of v2 source
00001B60	00001BC4			1180+	DC	A(RE25+32)	address of v3 source
00001B64	00000010			1181+	DC	A(16)	result length
00001B68	00001BA4			1182+REA25	DC	A(RE25)	result address
00001B70	00000000 00000000			1183+	DS	FD	gap
00001B78	00000000 00000000			1184+V1025	DS	XL16	V1 output
00001B80	00000000 00000000						
00001B88	00000000 00000000			1185+	DS	FD	gap
				1186+*			
00001B90				1187+X25	DS	0F	
00001B90	E760 8EA4 0806		000010A4	1188+	VL	V22, V1FUDGE	
00001B96	E760 FFFF 2845			1189+	VREPI	V22, - 1, 2	test instruction (dest is a source)
00001B9C	E760 5030 080E		00001B78	1190+	VST	V22, V1025	save v1 output
00001BA2	07FB			1191+	BR	R11	return
00001BA4				1192+RE25	DC	0F	xl16 expected result
00001BA4				1193+	DROP	R5	
00001BA4	FFFFFFFF FFFFFFFF			1194	DC	4FL4' - 1'	result
00001BAC	FFFFFFFF FFFFFFFF						
				1195			
				1196	VRI_A	VREPI, - 2, 2	
00001BB8				1197+	DS	0FD	
00001BB8		00001BB8		1198+	USING	*, R5	base for test data and test routine
00001BB8	00001C00			1199+T26	DC	A(X26)	address of test routine
00001BBC	001A			1200+	DC	H' 26'	test number
00001BBE	00			1201+	DC	X' 00'	
00001BBF	02			1202+	DC	HL1' 2'	m3 field
00001BC0	FFFE			1203+	DC	HL2' - 2'	i2 used
00001BC2	E5D9C5D7 C9404040			1204+	DC	CL8' VREPI'	instruction name
00001BCC	00001C24			1205+	DC	A(RE26+16)	address of v2 source
00001BD0	00001C34			1206+	DC	A(RE26+32)	address of v3 source
00001BD4	00000010			1207+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001BD8	00001C14			1208+REA26	DC	A(RE26)	result address
00001BE0	00000000 00000000			1209+	DS	FD	gap
00001BE8	00000000 00000000			1210+V1026	DS	XL16	V1 output
00001BF0	00000000 00000000						
00001BF8	00000000 00000000			1211+	DS	FD	gap
				1212+*			
00001C00				1213+X26	DS	0F	
00001C00	E760 8EA4 0806		000010A4	1214+	VL	V22, V1FUDGE	
00001C06	E760 FFFE 2845			1215+	VREPI	V22, - 2, 2	test instruction (dest is a source)
00001C0C	E760 5030 080E		00001BE8	1216+	VST	V22, V1026	save v1 output
00001C12	07FB			1217+	BR	R11	return
00001C14				1218+RE26	DC	0F	xl16 expected result
00001C14				1219+	DROP	R5	
00001C14	FFFFFFFFE FFFFFFFFE			1220	DC	4FL4' - 2'	result
00001C1C	FFFFFFFFE FFFFFFFFE						
				1221			
				1222	VRI_A	VREPI, - 720, 2	
00001C28				1223+	DS	0FD	
00001C28		00001C28		1224+	USING	*, R5	base for test data and test routine
00001C28	00001C70			1225+T27	DC	A(X27)	address of test routine
00001C2C	001B			1226+	DC	H' 27'	test number
00001C2E	00			1227+	DC	X' 00'	
00001C2F	02			1228+	DC	HL1' 2'	m3 field
00001C30	FD30			1229+	DC	HL2' - 720'	i2 used
00001C32	E5D9C5D7 C9404040			1230+	DC	CL8' VREPI'	instruction name
00001C3C	00001C94			1231+	DC	A(RE27+16)	address of v2 source
00001C40	00001CA4			1232+	DC	A(RE27+32)	address of v3 source
00001C44	00000010			1233+	DC	A(16)	result length
00001C48	00001C84			1234+REA27	DC	A(RE27)	result address
00001C50	00000000 00000000			1235+	DS	FD	gap
00001C58	00000000 00000000			1236+V1027	DS	XL16	V1 output
00001C60	00000000 00000000						
00001C68	00000000 00000000			1237+	DS	FD	gap
				1238+*			
00001C70				1239+X27	DS	0F	
00001C70	E760 8EA4 0806		000010A4	1240+	VL	V22, V1FUDGE	
00001C76	E760 FD30 2845			1241+	VREPI	V22, - 720, 2	test instruction (dest is a source)
00001C7C	E760 5030 080E		00001C58	1242+	VST	V22, V1027	save v1 output
00001C82	07FB			1243+	BR	R11	return
00001C84				1244+RE27	DC	0F	xl16 expected result
00001C84				1245+	DROP	R5	
00001C84	FFFFFD30 FFFFFD30			1246	DC	4FL4' - 720'	result
00001C8C	FFFFFD30 FFFFFD30						
				1247			
				1248	VRI_A	VREPI, - 31456, 2	
00001C98				1249+	DS	0FD	
00001C98		00001C98		1250+	USING	*, R5	base for test data and test routine
00001C98	00001CE0			1251+T28	DC	A(X28)	address of test routine
00001C9C	001C			1252+	DC	H' 28'	test number
00001C9E	00			1253+	DC	X' 00'	
00001C9F	02			1254+	DC	HL1' 2'	m3 field
00001CA0	8520			1255+	DC	HL2' - 31456'	i2 used
00001CA2	E5D9C5D7 C9404040			1256+	DC	CL8' VREPI'	instruction name
00001CAC	00001D04			1257+	DC	A(RE28+16)	address of v2 source
00001CB0	00001D14			1258+	DC	A(RE28+32)	address of v3 source
00001CB4	00000010			1259+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001CB8	00001CF4			1260+REA28	DC	A(RE28)	result address
00001CC0	00000000 00000000			1261+	DS	FD	gap
00001CC8	00000000 00000000			1262+V1028	DS	XL16	V1 output
00001CD0	00000000 00000000						
00001CD8	00000000 00000000			1263+	DS	FD	gap
				1264+*			
00001CE0				1265+X28	DS	0F	
00001CE0	E760 8EA4 0806		000010A4	1266+	VL	V22, V1FUDGE	
00001CE6	E760 8520 2845			1267+	VREPI	V22, - 31456, 2	test instruction (dest is a source)
00001CEC	E760 5030 080E		00001CC8	1268+	VST	V22, V1028	save v1 output
00001CF2	07FB			1269+	BR	R11	return
00001CF4				1270+RE28	DC	0F	xl16 expected result
00001CF4				1271+	DROP	R5	
00001CF4	FFFF8520 FFFF8520			1272	DC	4FL4' - 31456'	result
00001CFC	FFFF8520 FFFF8520						
				1273			
				1274 *Doubleword			
				1275	VRI_A	VREPI, 0, 3	
00001D08				1276+	DS	0FD	
00001D08		00001D08		1277+	USING	*, R5	base for test data and test routine
00001D08	00001D50			1278+T29	DC	A(X29)	address of test routine
00001D0C	001D			1279+	DC	H' 29'	test number
00001D0E	00			1280+	DC	X' 00'	
00001D0F	03			1281+	DC	HL1' 3'	m3 field
00001D10	0000			1282+	DC	HL2' 0'	i2 used
00001D12	E5D9C5D7 C9404040			1283+	DC	CL8' VREPI'	instruction name
00001D1C	00001D74			1284+	DC	A(RE29+16)	address of v2 source
00001D20	00001D84			1285+	DC	A(RE29+32)	address of v3 source
00001D24	00000010			1286+	DC	A(16)	result length
00001D28	00001D64			1287+REA29	DC	A(RE29)	result address
00001D30	00000000 00000000			1288+	DS	FD	gap
00001D38	00000000 00000000			1289+V1029	DS	XL16	V1 output
00001D40	00000000 00000000						
00001D48	00000000 00000000			1290+	DS	FD	gap
				1291+*			
00001D50				1292+X29	DS	0F	
00001D50	E760 8EA4 0806		000010A4	1293+	VL	V22, V1FUDGE	
00001D56	E760 0000 3845			1294+	VREPI	V22, 0, 3	test instruction (dest is a source)
00001D5C	E760 5030 080E		00001D38	1295+	VST	V22, V1029	save v1 output
00001D62	07FB			1296+	BR	R11	return
00001D64				1297+RE29	DC	0F	xl16 expected result
00001D64				1298+	DROP	R5	
00001D64	00000000 00000000			1299	DC	2DL8' 0'	result
00001D6C	00000000 00000000						
				1300			
				1301	VRI_A	VREPI, 1, 3	
00001D78				1302+	DS	0FD	
00001D78		00001D78		1303+	USING	*, R5	base for test data and test routine
00001D78	00001DC0			1304+T30	DC	A(X30)	address of test routine
00001D7C	001E			1305+	DC	H' 30'	test number
00001D7E	00			1306+	DC	X' 00'	
00001D7F	03			1307+	DC	HL1' 3'	m3 field
00001D80	0001			1308+	DC	HL2' 1'	i2 used
00001D82	E5D9C5D7 C9404040			1309+	DC	CL8' VREPI'	instruction name
00001D8C	00001DE4			1310+	DC	A(RE30+16)	address of v2 source
00001D90	00001DF4			1311+	DC	A(RE30+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001D94	00000010			1312+	DC	A(16)	result length
00001D98	00001DD4			1313+REA30	DC	A(RE30)	result address
00001DA0	00000000 00000000			1314+	DS	FD	gap
00001DA8	00000000 00000000			1315+V1030	DS	XL16	V1 output
00001DB0	00000000 00000000						
00001DB8	00000000 00000000			1316+	DS	FD	gap
				1317+*			
00001DC0				1318+X30	DS	0F	
00001DC0	E760 8EA4 0806		000010A4	1319+	VL	V22, V1FUDGE	
00001DC6	E760 0001 3845			1320+	VREPI	V22, 1, 3	test instruction (dest is a source)
00001DCC	E760 5030 080E		00001DA8	1321+	VST	V22, V1030	save v1 output
00001DD2	07FB			1322+	BR	R11	return
00001DD4				1323+RE30	DC	0F	xl16 expected result
00001DD4				1324+	DROP	R5	
00001DD4	00000000 00000001			1325	DC	2DL8' 1'	result
00001DDC	00000000 00000001						
				1326			
00001DE8				1327	VRI_A	VREPI, 2, 3	
00001DE8		00001DE8		1328+	DS	0FD	
00001DE8	00001E30			1329+	USING	*, R5	base for test data and test routine
00001DEC	001F			1330+T31	DC	A(X31)	address of test routine
00001DEE	00			1331+	DC	H' 31'	test number
00001DEF	03			1332+	DC	X' 00'	
00001DF0	0002			1333+	DC	HL1' 3'	m3 field
00001DF2	E5D9C5D7 C9404040			1334+	DC	HL2' 2'	i2 used
00001DFC	00001E54			1335+	DC	CL8' VREPI'	instruction name
00001E00	00001E64			1336+	DC	A(RE31+16)	address of v2 source
00001E04	00000010			1337+	DC	A(RE31+32)	address of v3 source
00001E08	00001E44			1338+	DC	A(16)	result length
00001E08	00001E44			1339+REA31	DC	A(RE31)	result address
00001E10	00000000 00000000			1340+	DS	FD	gap
00001E18	00000000 00000000			1341+V1031	DS	XL16	V1 output
00001E20	00000000 00000000						
00001E28	00000000 00000000			1342+	DS	FD	gap
				1343+*			
00001E30				1344+X31	DS	0F	
00001E30	E760 8EA4 0806		000010A4	1345+	VL	V22, V1FUDGE	
00001E36	E760 0002 3845			1346+	VREPI	V22, 2, 3	test instruction (dest is a source)
00001E3C	E760 5030 080E		00001E18	1347+	VST	V22, V1031	save v1 output
00001E42	07FB			1348+	BR	R11	return
00001E44				1349+RE31	DC	0F	xl16 expected result
00001E44				1350+	DROP	R5	
00001E44	00000000 00000002			1351	DC	2DL8' 2'	result
00001E4C	00000000 00000002						
				1352			
00001E58				1353	VRI_A	VREPI, 99, 3	
00001E58		00001E58		1354+	DS	0FD	
00001E58	00001EA0			1355+	USING	*, R5	base for test data and test routine
00001E5C	0020			1356+T32	DC	A(X32)	address of test routine
00001E5E	00			1357+	DC	H' 32'	test number
00001E5F	03			1358+	DC	X' 00'	
00001E60	0063			1359+	DC	HL1' 3'	m3 field
00001E62	E5D9C5D7 C9404040			1360+	DC	HL2' 99'	i2 used
00001E62	E5D9C5D7 C9404040			1361+	DC	CL8' VREPI'	instruction name
00001E6C	00001EC4			1362+	DC	A(RE32+16)	address of v2 source
00001E70	00001ED4			1363+	DC	A(RE32+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001E74	00000010			1364+	DC	A(16)	result length
00001E78	00001EB4			1365+REA32	DC	A(RE32)	result address
00001E80	00000000 00000000			1366+	DS	FD	gap
00001E88	00000000 00000000			1367+V1032	DS	XL16	V1 output
00001E90	00000000 00000000						
00001E98	00000000 00000000			1368+	DS	FD	gap
				1369+*			
00001EA0				1370+X32	DS	0F	
00001EA0	E760 8EA4 0806		000010A4	1371+	VL	V22, V1FUDGE	
00001EA6	E760 0063 3845			1372+	VREPI	V22, 99, 3	test instruction (dest is a source)
00001EAC	E760 5030 080E		00001E88	1373+	VST	V22, V1032	save v1 output
00001EB2	07FB			1374+	BR	R11	return
00001EB4				1375+RE32	DC	0F	xl16 expected result
00001EB4				1376+	DROP	R5	
00001EB4	00000000 00000063			1377	DC	2DL8' 99'	result
00001EBC	00000000 00000063						
				1378			
00001EC8				1379	VRI_A	VREPI, 9999, 3	
00001EC8		00001EC8		1380+	DS	0FD	
00001EC8	00001F10			1381+	USING	*, R5	base for test data and test routine
00001ECC	0021			1382+T33	DC	A(X33)	address of test routine
00001ECE	00			1383+	DC	H' 33'	test number
00001ECF	03			1384+	DC	X' 00'	
00001ED0	270F			1385+	DC	HL1' 3'	m3 field
00001ED2	E5D9C5D7 C9404040			1386+	DC	HL2' 9999'	i2 used
00001EDC	00001F34			1387+	DC	CL8' VREPI'	instruction name
00001EE0	00001F44			1388+	DC	A(RE33+16)	address of v2 source
00001EE4	00000010			1389+	DC	A(RE33+32)	address of v3 source
00001EE8	00001F24			1390+	DC	A(16)	result length
00001EF0	00000000 00000000			1391+REA33	DC	A(RE33)	result address
00001EF8	00000000 00000000			1392+	DS	FD	gap
00001F00	00000000 00000000			1393+V1033	DS	XL16	V1 output
00001F08	00000000 00000000						
				1394+	DS	FD	gap
				1395+*			
00001F10				1396+X33	DS	0F	
00001F10	E760 8EA4 0806		000010A4	1397+	VL	V22, V1FUDGE	
00001F16	E760 270F 3845			1398+	VREPI	V22, 9999, 3	test instruction (dest is a source)
00001F1C	E760 5030 080E		00001EF8	1399+	VST	V22, V1033	save v1 output
00001F22	07FB			1400+	BR	R11	return
00001F24				1401+RE33	DC	0F	xl16 expected result
00001F24				1402+	DROP	R5	
00001F24	00000000 0000270F			1403	DC	2DL8' 9999'	result
00001F2C	00000000 0000270F						
				1404			
00001F38				1405	VRI_A	VREPI, - 1, 3	
00001F38		00001F38		1406+	DS	0FD	
00001F38	00001F80			1407+	USING	*, R5	base for test data and test routine
00001F3C	0022			1408+T34	DC	A(X34)	address of test routine
00001F3E	00			1409+	DC	H' 34'	test number
00001F3F	03			1410+	DC	X' 00'	
00001F40	FFFF			1411+	DC	HL1' 3'	m3 field
00001F42	E5D9C5D7 C9404040			1412+	DC	HL2' - 1'	i2 used
00001F4C	00001FA4			1413+	DC	CL8' VREPI'	instruction name
00001F50	00001FB4			1414+	DC	A(RE34+16)	address of v2 source
				1415+	DC	A(RE34+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001F54	00000010			1416+	DC	A(16)	result length
00001F58	00001F94			1417+REA34	DC	A(RE34)	result address
00001F60	00000000 00000000			1418+	DS	FD	gap
00001F68	00000000 00000000			1419+V1034	DS	XL16	V1 output
00001F70	00000000 00000000						
00001F78	00000000 00000000			1420+	DS	FD	gap
				1421+*			
00001F80				1422+X34	DS	0F	
00001F80	E760 8EA4 0806		000010A4	1423+	VL	V22, V1FUDGE	
00001F86	E760 FFFF 3845			1424+	VREPI	V22, - 1, 3	test instruction (dest is a source)
00001F8C	E760 5030 080E		00001F68	1425+	VST	V22, V1034	save v1 output
00001F92	07FB			1426+	BR	R11	return
00001F94				1427+RE34	DC	0F	xl16 expected result
00001F94				1428+	DROP	R5	
00001F94	FFFFFFFF FFFFFFFF			1429	DC	2DL8' - 1'	result t
00001F9C	FFFFFFFF FFFFFFFF						
				1430			
00001FA8				1431	VRI_A	VREPI, - 2, 3	
00001FA8		00001FA8		1432+	DS	0FD	
00001FA8	00001FF0			1433+	USING	*, R5	base for test data and test routine
00001FAC	0023			1434+T35	DC	A(X35)	address of test routine
00001FAE	00			1435+	DC	H' 35'	test number
00001FAE	00			1436+	DC	X' 00'	
00001FAF	03			1437+	DC	HL1' 3'	m3 field
00001FB0	FFFE			1438+	DC	HL2' - 2'	i2 used
00001FB2	E5D9C5D7 C9404040			1439+	DC	CL8' VREPI'	instruction name
00001FBC	00002014			1440+	DC	A(RE35+16)	address of v2 source
00001FC0	00002024			1441+	DC	A(RE35+32)	address of v3 source
00001FC4	00000010			1442+	DC	A(16)	result length
00001FC8	00002004			1443+REA35	DC	A(RE35)	result address
00001FD0	00000000 00000000			1444+	DS	FD	gap
00001FD8	00000000 00000000			1445+V1035	DS	XL16	V1 output
00001FE0	00000000 00000000						
00001FE8	00000000 00000000			1446+	DS	FD	gap
				1447+*			
00001FF0				1448+X35	DS	0F	
00001FF0	E760 8EA4 0806		000010A4	1449+	VL	V22, V1FUDGE	
00001FF6	E760 FFFE 3845			1450+	VREPI	V22, - 2, 3	test instruction (dest is a source)
00001FFC	E760 5030 080E		00001FD8	1451+	VST	V22, V1035	save v1 output
00002002	07FB			1452+	BR	R11	return
00002004				1453+RE35	DC	0F	xl16 expected result
00002004				1454+	DROP	R5	
00002004	FFFFFFFF FFFFFFFF			1455	DC	2DL8' - 2'	result t
0000200C	FFFFFFFF FFFFFFFF						
				1456			
00002018				1457	VRI_A	VREPI, - 720, 3	
00002018		00002018		1458+	DS	0FD	
00002018	00002060			1459+	USING	*, R5	base for test data and test routine
0000201C	0024			1460+T36	DC	A(X36)	address of test routine
0000201E	00			1461+	DC	H' 36'	test number
0000201E	00			1462+	DC	X' 00'	
0000201F	03			1463+	DC	HL1' 3'	m3 field
00002020	FD30			1464+	DC	HL2' - 720'	i2 used
00002022	E5D9C5D7 C9404040			1465+	DC	CL8' VREPI'	instruction name
0000202C	00002084			1466+	DC	A(RE36+16)	address of v2 source
00002030	00002094			1467+	DC	A(RE36+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002034	00000010			1468+	DC	A(16)	result length
00002038	00002074			1469+REA36	DC	A(RE36)	result address
00002040	00000000 00000000			1470+	DS	FD	gap
00002048	00000000 00000000			1471+V1036	DS	XL16	V1 output
00002050	00000000 00000000						
00002058	00000000 00000000			1472+	DS	FD	gap
				1473+*			
00002060				1474+X36	DS	0F	
00002060	E760 8EA4 0806		000010A4	1475+	VL	V22, V1FUDGE	
00002066	E760 FD30 3845			1476+	VREPI	V22, - 720, 3	test instruction (dest is a source)
0000206C	E760 5030 080E		00002048	1477+	VST	V22, V1036	save v1 output
00002072	07FB			1478+	BR	R11	return
00002074				1479+RE36	DC	0F	xl16 expected result
00002074				1480+	DROP	R5	
00002074	FFFFFFFF FFFFD30			1481	DC	2DL8' - 720'	result t
0000207C	FFFFFFFF FFFFD30						
				1482			
00002088				1483	VRI_A	VREPI, - 31456, 3	
00002088		00002088		1484+	DS	0FD	
00002088	000020D0			1485+	USING	*, R5	base for test data and test routine
0000208C	0025			1486+T37	DC	A(X37)	address of test routine
0000208E	00			1487+	DC	H' 37'	test number
0000208E	00			1488+	DC	X' 00'	
0000208F	03			1489+	DC	HL1' 3'	m3 field
00002090	8520			1490+	DC	HL2' - 31456'	i2 used
00002092	E5D9C5D7 C9404040			1491+	DC	CL8' VREPI'	instruction name
0000209C	000020F4			1492+	DC	A(RE37+16)	address of v2 source
000020A0	00002104			1493+	DC	A(RE37+32)	address of v3 source
000020A4	00000010			1494+	DC	A(16)	result length
000020A8	000020E4			1495+REA37	DC	A(RE37)	result address
000020B0	00000000 00000000			1496+	DS	FD	gap
000020B8	00000000 00000000			1497+V1037	DS	XL16	V1 output
000020C0	00000000 00000000						
000020C8	00000000 00000000			1498+	DS	FD	gap
				1499+*			
000020D0				1500+X37	DS	0F	
000020D0	E760 8EA4 0806		000010A4	1501+	VL	V22, V1FUDGE	
000020D6	E760 8520 3845			1502+	VREPI	V22, - 31456, 3	test instruction (dest is a source)
000020DC	E760 5030 080E		000020B8	1503+	VST	V22, V1037	save v1 output
000020E2	07FB			1504+	BR	R11	return
000020E4				1505+RE37	DC	0F	xl16 expected result
000020E4				1506+	DROP	R5	
000020E4	FFFFFFFF FFFF8520			1507	DC	2DL8' - 31456'	result t
000020EC	FFFFFFFF FFFF8520						
				1508			
				1509			
				1510			
000020F4	00000000			1511	DC	F' 0'	END OF TABLE
000020F8	00000000			1512	DC	F' 0'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				1514 *
				1515 * table of pointers to individual load test
				1516 *
000020FC				1517 E7TESTS DS OF
				1518 PTTABLE
000020FC				1519+TTABLE DS OF
000020FC	000010C8			1520+ DC A(T1)
00002100	00001138			1521+ DC A(T2)
00002104	000011A8			1522+ DC A(T3)
00002108	00001218			1523+ DC A(T4)
0000210C	00001288			1524+ DC A(T5)
00002110	000012F8			1525+ DC A(T6)
00002114	00001368			1526+ DC A(T7)
00002118	000013D8			1527+ DC A(T8)
0000211C	00001448			1528+ DC A(T9)
00002120	000014B8			1529+ DC A(T10)
00002124	00001528			1530+ DC A(T11)
00002128	00001598			1531+ DC A(T12)
0000212C	00001608			1532+ DC A(T13)
00002130	00001678			1533+ DC A(T14)
00002134	000016E8			1534+ DC A(T15)
00002138	00001758			1535+ DC A(T16)
0000213C	000017C8			1536+ DC A(T17)
00002140	00001838			1537+ DC A(T18)
00002144	000018A8			1538+ DC A(T19)
00002148	00001918			1539+ DC A(T20)
0000214C	00001988			1540+ DC A(T21)
00002150	000019F8			1541+ DC A(T22)
00002154	00001A68			1542+ DC A(T23)
00002158	00001AD8			1543+ DC A(T24)
0000215C	00001B48			1544+ DC A(T25)
00002160	00001BB8			1545+ DC A(T26)
00002164	00001C28			1546+ DC A(T27)
00002168	00001C98			1547+ DC A(T28)
0000216C	00001D08			1548+ DC A(T29)
00002170	00001D78			1549+ DC A(T30)
00002174	00001DE8			1550+ DC A(T31)
00002178	00001E58			1551+ DC A(T32)
0000217C	00001EC8			1552+ DC A(T33)
00002180	00001F38			1553+ DC A(T34)
00002184	00001FA8			1554+ DC A(T35)
00002188	00002018			1555+ DC A(T36)
0000218C	00002088			1556+ DC A(T37)
				1557+*
00002190	00000000			1558+ DC A(0)
00002194	00000000			1559+ DC A(0)
				1560
00002198	00000000			1561 DC F' 0'
0000219C	00000000			1562 DC F' 0'

END OF TABLE

END OF TABLE

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				1564	*****		
				1565	* Register equates		
				1566	*****		
		00000000	00000001	1568 R0	EQU	0	
		00000001	00000001	1569 R1	EQU	1	
		00000002	00000001	1570 R2	EQU	2	
		00000003	00000001	1571 R3	EQU	3	
		00000004	00000001	1572 R4	EQU	4	
		00000005	00000001	1573 R5	EQU	5	
		00000006	00000001	1574 R6	EQU	6	
		00000007	00000001	1575 R7	EQU	7	
		00000008	00000001	1576 R8	EQU	8	
		00000009	00000001	1577 R9	EQU	9	
		0000000A	00000001	1578 R10	EQU	10	
		0000000B	00000001	1579 R11	EQU	11	
		0000000C	00000001	1580 R12	EQU	12	
		0000000D	00000001	1581 R13	EQU	13	
		0000000E	00000001	1582 R14	EQU	14	
		0000000F	00000001	1583 R15	EQU	15	
				1585	*****		
				1586	* Register equates		
				1587	*****		
		00000000	00000001	1589 V0	EQU	0	
		00000001	00000001	1590 V1	EQU	1	
		00000002	00000001	1591 V2	EQU	2	
		00000003	00000001	1592 V3	EQU	3	
		00000004	00000001	1593 V4	EQU	4	
		00000005	00000001	1594 V5	EQU	5	
		00000006	00000001	1595 V6	EQU	6	
		00000007	00000001	1596 V7	EQU	7	
		00000008	00000001	1597 V8	EQU	8	
		00000009	00000001	1598 V9	EQU	9	
		0000000A	00000001	1599 V10	EQU	10	
		0000000B	00000001	1600 V11	EQU	11	
		0000000C	00000001	1601 V12	EQU	12	
		0000000D	00000001	1602 V13	EQU	13	
		0000000E	00000001	1603 V14	EQU	14	
		0000000F	00000001	1604 V15	EQU	15	
		00000010	00000001	1605 V16	EQU	16	
		00000011	00000001	1606 V17	EQU	17	
		00000012	00000001	1607 V18	EQU	18	
		00000013	00000001	1608 V19	EQU	19	
		00000014	00000001	1609 V20	EQU	20	
		00000015	00000001	1610 V21	EQU	21	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA16	A	00001778	4	947		
REA17	A	000017E8	4	973		
REA18	A	00001858	4	999		
REA19	A	000018C8	4	1025		
REA2	A	00001158	4	582		
REA20	A	00001938	4	1052		
REA21	A	000019A8	4	1078		
REA22	A	00001A18	4	1104		
REA23	A	00001A88	4	1130		
REA24	A	00001AF8	4	1156		
REA25	A	00001B68	4	1182		
REA26	A	00001BD8	4	1208		
REA27	A	00001C48	4	1234		
REA28	A	00001CB8	4	1260		
REA29	A	00001D28	4	1287		
REA3	A	000011C8	4	608		
REA30	A	00001D98	4	1313		
REA31	A	00001E08	4	1339		
REA32	A	00001E78	4	1365		
REA33	A	00001EE8	4	1391		
REA34	A	00001F58	4	1417		
REA35	A	00001FC8	4	1443		
REA36	A	00002038	4	1469		
REA37	A	000020A8	4	1495		
REA4	A	00001238	4	634		
REA5	A	000012A8	4	660		
REA6	A	00001318	4	686		
REA7	A	00001388	4	712		
REA8	A	000013F8	4	738		
REA9	A	00001468	4	765		
READDR	A	00000020	4	448	218	
REG2LOW	U	000000DD	1	386		
REG2PATT	U	AABBCCDD	1	385		
RELEN	A	0000001C	4	447		
RPTDWSAV	D	000003D0	8	308	295	299
RPTERROR	I	00000326	4	256	231	
RPTSAVE	F	000003C8	4	305	256	302
RPTSVR5	F	000003CC	4	306	257	301
SKL0001	U	0000004E	1	177	193	
SKT0001	C	0000022A	20	174	177	194
SVOLDPSW	U	00000140	0	113		
T1	A	000010C8	4	547	1520	
T10	A	000014B8	4	782	1529	
T11	A	00001528	4	808	1530	
T12	A	00001598	4	834	1531	
T13	A	00001608	4	860	1532	
T14	A	00001678	4	886	1533	
T15	A	000016E8	4	912	1534	
T16	A	00001758	4	938	1535	
T17	A	000017C8	4	964	1536	
T18	A	00001838	4	990	1537	
T19	A	000018A8	4	1016	1538	
T2	A	00001138	4	573	1521	
T20	A	00001918	4	1043	1539	
T21	A	00001988	4	1069	1540	
T22	A	000019F8	4	1095	1541	

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	8608	0000- 219F	0000- 219F
Regi on		8608	0000- 219F	0000- 219F
CSECT	ZVE7TST	8608	0000- 219F	0000- 219F

STMT	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e7-21-VREPI.asm
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**** NO ERRORS FOUND ****